**ELIZADE UNIVERSITY, ILARA-MOKIN, ONDO STATE**

**FACULTY OF ENGINEERING**

**DEPARTMENT OF COMPUTER ENGINEERING**

**FIRST SEMESTER EXAMINATION, 2023/2024 ACADEMIC SESSION**

**COURSE TITLE: DIGITAL SYSTEM DESIGN WITH VHDL**

**COURSE CODE: CPE351/ECE 521 (2 UNITS)**

**EXAMINATION DATE:**

**TIME ALLOWED: 2 HOURS**

**INSTRUCTIONS:**

1. ANSWER ANY FOUR (4) QUESTIONS
2. SEVERE PENALTIES APPLY FOR MISCONDUCT, CHEATING, POSSESSION OF UNAUTHORIZED MATERIALS DURING EXAM.
3. YOU ARE **NOT** ALLOWED TO BORROW ANY WRITING MATERIALS DURING THE EXAMINATION.

**Question 1**

1. Discuss what you understand by sequential digital circuits. **2 Marks**
2. Discuss the implementation of an SR latch with two NAND gates. Includes the circuit diagram, and its truth table to illustrate the working principles of the circuit. **5 marks**
3. 

Figure 1: Timing diagram of an SR Latch

1. Given Figure 1 timing diagram of an SR latch, sketch the outputs of the bistable device. **5 marks**
2. Briefly discuss the three forms of multi-vibrator **3 marks**

**Question 2**

1. State three (3) the areas of application of flip-flop in our society and the world at large.

 **3 Marks**

1. What is the limitation of JK flip-flop? **1 Mark**
2. Based on your knowledge in Digital System Design with VHDL class, provide a solution to the problem with JK flip-flop, including your solution's circuit diagram and truth table. **8 Marks**
3. Write the equation of Figure 2, and simplify the equation to the simplest form. **3 Marks**



**Figure 2: Logic circuit**

**Question 3**

1. What did you understand by Shift Registers? **2 Marks**
2. Identify the three (3) application areas of digital counters in developing real-time digital systems in our cities today. **3 Marks**
3. Design the circuit and state diagrams of a modulo 12 asynchronous counter. **6 Marks**
4. State four (4) advantages of VHDL **4 Marks**

**Question 4**

1. Discuss what you understand by the acronym HDL **1 Mark**
2. Sketch and briefly explain the design flow of a VHDL program **6 Marks**
3. Write a complete program in VHDL for the logic circuit in Figure 3, using the behavioral modelling style. The entity name should follow this format **name of the circuit in figure 3\_Your Matric No** e.g. **ANDGATE\_EU1803041985** and architecture name **CPE351\_lastname** e.g. **Arch\_Adeleke.**



 **Figure 3: A combinational logic circuit 8 Marks**

**Question 5**

1. State the procedure for setting up a new project in Altera Quartus software **2 Marks**
2. Design a Moore machine for a binary input sequence, such that if it has a substring 111 the machine output is A., if the input has substring 110 its output is B otherwise its output is C. **6 Marks**
3. Discuss the problem in the ICs industry that led to the development of VHDL **3 Marks**
4. Sketch the block diagram of a **PIPO** shift register **4 Marks**

**Question 6**

1. With the aid of block diagrams, differentiate between a Moore State Machine and a Mealy State Machine. **2 Marks**
2. Demonstrate the working principles of the 4-bit SISO shift register with input string “1011”. **5 Marks**
3. Identify the three libraries usually used in all VHDL codes **3 Marks**
4. State 5 precautions you must take while working on Digital System Design Laboratory practical. **5 Marks**

**Wishing you good success in Jesus’ name**